

Preliminary **AD8541/42/44**

FEATURES

Single-Supply Operation: 2.7 to 5.5 Volts
Low Supply Current: 40 μ A/amplifier
Wide Bandwidth: 500 kHz
Slew Rate: 0.5 V/ μ s
No Phase Reversal
Low Input Currents: 4 pA
Unity Gain Stable

APPLICATIONS

Medical Instrumentation
Integrators
ASIC Input or Output Amplifier
Piezoelectric Transducer Amplifier

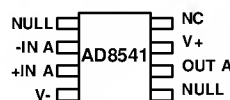
GENERAL DESCRIPTION

The AD8541, AD8542 and AD8544 are single, dual and quad **rail-to-rail input and output** single-supply amplifiers featuring ultra low bias current. All are guaranteed to operate from a **+3 volt single supply** as well as a +5 volt supply.

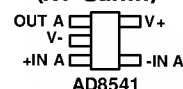
Very low input bias currents enable the AD854X to be used for integrators, diode amplification or applications with a very high source impedance. Supply current is only 40 μ A per amplifier, ideal for battery operation or designs where power must be supplied across an isolation barrier. High output current combined with low power and no phase reversal makes the AD854x family a good choice for 4 to 20 mA applications.

Rail-to-rail inputs and outputs are beneficial to designers buffering CMOS DACs, ASICs or other wide output swing devices in single-supply systems.

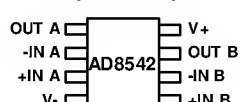
**8-Lead SO
(R Suffix)**



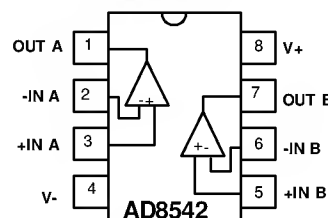
**5-Lead SOT
(RT Suffix)**



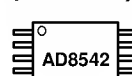
**8-Lead SO
(R Suffix)**



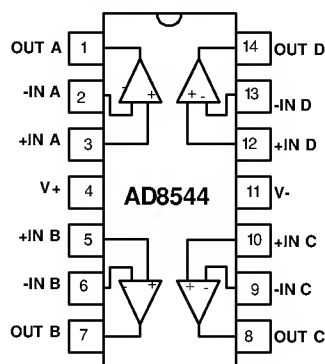
**8-Lead Epoxy DIP
(N Suffix)**



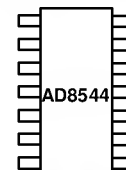
**8-Lead TSSOP
(RU Suffix)**



**14-Lead Epoxy DIP
(N Suffix)**



**14-Lead
Narrow-Body SO
(N Suffix)**



**14-Lead TSSOP
(RU Suffix)**



Note: Pin orientation is equivalent for each package variation

The AD8541, AD8542 and AD8544 are specified over the extended industrial (-40° to $+125^{\circ}$ C) temperature range. The AD8541 is available in SO-8 and SOT23-5 packages. The AD8542 is available in 8-pin plastic DIPs, SO-8 and 8-lead TSSOP surface mount packages. The AD8544 is available in 14-pin plastic DIPs, narrow SO-14 and 14-lead TSSOP surface mount packages. All TSSOP and SOT versions are available in tape and reel only.

REV. 0

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AD8541/42/44

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ELECTRICAL CHARACTERISTICS (@ $V_S = +3.0V$, $V_{CM} = 1.5V$, $T_A = +25^\circ C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ \leq T_A \leq +85^\circ C$		1	5	mV
Input Bias Current	I_B	$-40^\circ \leq T_A \leq +85^\circ C$		0.1	4	pA
Input Offset Current	I_{OS}	$-40^\circ \leq T_A \leq +85^\circ C$		0.1	2	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0$ to $3V$	65	75		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 100k\Omega$, $V_O = 0.5$ to $2.5V$	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		$\mu V/^\circ C$
Bias Current Drift	$\Delta I_B/\Delta T$					fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$					fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = \mu A$ $-40^\circ C \leq T_A \leq +85^\circ C$	2.85 2.8	2.92		V
Output Voltage Low	V_{OL}	$I_L = \mu A$ $-40^\circ C \leq T_A \leq +85^\circ C$		60	100 125	mV
Output Current	I_{OUT}			± 10		mA
Closed Loop Output Impedance	Z_{out}	$f = 1MHz$, $A_V = 1$				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.5V$ to $5.5V$	70	85		dB
Supply Current/Amplifier	I_{SY}	$V_O = 0V$ $-40^\circ \leq T_A \leq +85^\circ C$		35	50 70	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100k\Omega$	0.4	0.6		V/ μs
Settling Time	t_s	To 0.01%		8		μs
Gain Bandwidth Product	GBP			500		kHz
Phase Margin	ϕ_o					degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	$f = 1kHz$		100		nV/ \sqrt{Hz}
Voltage Noise Density	e_n	$f = 10kHz$		90		nV/ \sqrt{Hz}
Current Noise Density	i_n					pA/ \sqrt{Hz}

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = +5.0V$, $V_{CM} = 2.5V$, $T_A = +25^\circ C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ \leq T_A \leq +85^\circ C$		1	5	mV
Input Bias Current	I_B	$-40^\circ \leq T_A \leq +85^\circ C$		0.1	4	pA
Input Offset Current	I_{OS}	$-40^\circ \leq T_A \leq +85^\circ C$		0.1	2	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0$ to $5V$	75	80		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 100k\Omega$, $V_o = 0.5$ to $4.5V$	300			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ \leq T_A \leq +85^\circ C$		2		$\mu V/^\circ C$
Bias Current Drift	$\Delta I_B/\Delta T$					fA/ $^\circ C$
Offset Current Drift	$\Delta I_{OS}/\Delta T$					fA/ $^\circ C$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 10\mu A$ $-40^\circ C \leq T_A \leq +85^\circ C$	4.9 4.85	4.94		V V
Output Voltage Low	V_{OL}	$I_L = 10\mu A$ $-40^\circ C \leq T_A \leq +85^\circ C$		50	100 125	mV mV
Output Current	I_{OUT}			± 25		mA
Closed Loop Output Impedance	Z_{out}	$f = 1kHz$, $A_V = 1$				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.5V$ to $5.5V$	70	85		dB
Supply Current/Amplifier	I_{SY}	$V_o = 0V$ $-40^\circ \leq T_A \leq +85^\circ C$		40	60 80	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 100k\Omega$, $C_L = 200pF$	0.5	0.7		V/ μs
Full-Power Bandwidth	BW_p	1% Distortion				kHz
Settling Time	t_s	To 0.01%		6		μs
Gain Bandwidth Product	GBP			700		kHz
Phase Margin	ϕ_o					degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	$f = 1 kHz$		90		nV/ \sqrt{Hz}
Voltage Noise Density	e_n	$f = 10 kHz$		80		nV/ \sqrt{Hz}
Current Noise Density	i_n					pA/ \sqrt{Hz}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S) +6V
 Input Voltage Gnd to V_S
 Differential Input Voltage¹ $\pm 6V$
 Storage Temperature Range
 N, R, RT, RU Package -65°C to +150°C
 Operating Temperature Range
 AD8541, AD8542, AD8544 -40°C to +85°C
 Junction Temperature Range
 N, R, RT, RU Package -65°C to +150°C
 Lead Temperature Range (Soldering, 60 Sec) +300°C

PACKAGE INFORMATION

Package Type	θ_{JA} ²	θ_{JC}	Units
5-Lead SOT-23 (RT)			°C/W
8-Pin SOIC (R)	158	43	°C/W
8-Pin TSSOP (RU)	240	43	°C/W
14-Pin Plastic DIP (N)	83	39	°C/W
14-Pin SOIC (R)	120	36	°C/W
14-Pin TSSOP (RU)			°C/W

NOTES

¹ For supplies less than +6 volts, the differential input voltage is equal to $\pm V_S$.

² θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered onto a circuit board for surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8541AR	-40°C to +85°C	8-Pin SOIC	SO-8
AD8541ART†	-40°C to +85°C	5-Lead SOT-23	RT-5
AD8542AR	-40°C to +85°C	8-Pin SOIC	SO-8
AD8542AN	-40°C to +85°C	8-Pin Plastic DIP	N-8
AD8542ARU*	-40°C to +85°C	8-Pin TSSOP	RU-8
AD8544AR	-40°C to +85°C	14-Pin SOIC	SO-14
AD8544AN	-40°C to +85°C	14-Pin Plastic DIP	N-14
AD8544ARU*	-40°C to +85°C	14-Pin TSSOP	RU-14

* Available in 2,500 piece reels only.

† Available in 3,000 or 10,000 piece reels.